

MEMORY INTERFACE SYSTEM

ABSTRACT

The invention relates to a semiconductor memory device and, more particularly, to an
5 interface system for a semiconductor memory device. The interface includes a transmitter
capable of encoding first and second input signals as a plural-bit symbol signal responsive to
first and second clocks, respectively, the first clock being out of phase from the second clock.
And the interface includes a receiver capable of generating first and second output signals by
decoding the symbol signal responsive to third and fourth clocks, respectively. Other
10 embodiments are illustrated and described.